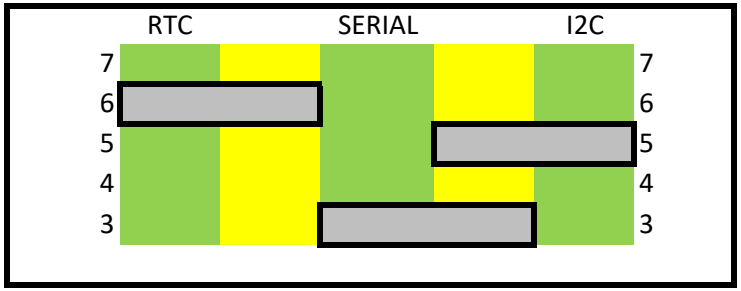
System Support II Jumper Settings

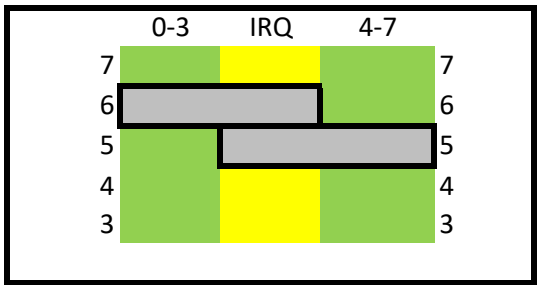
Board Rev "L" 3/7/2023

Jumper		Default	
Bus control			
JP1	WRITE	LATCH	Use either the LATCHed IOW, or the raw signal from the BUS.
JP2	READ	LATCH	Use either the LATCHEed IOR, or the raw signal from the BUS.
Digitalker ROM			
JP3	ROM Type	28C	Select either 27C (UV eraseable) or 28C (electrically eraseable) ROM for the Digitalker ROM at U18
JP4	ROM Enable	ON	Power control for U18: ON is continuous, EN is on only when Digitalker requests data.
Serial port configuration			
JP5	Ext Loop	OFF	Loops DSR to DTR as seen at externally attached device
JP6	Int Loop	OFF	Loops DSR to DTR as seen at H8 interface to UART
JP11	SIN	EXT	SerialIN connects to either EXTernal device at headers or EMIC2 at J22
JP12	SOUT	EXT	SerialOUT connects to either EXTernal device at headers or EMIC2 at J22
+3.3V Power Source			
JP10	I2C3V	U39	Source of 3.3v power to I2C: VDIP (if installed) or U39 (78L33)
PCA9685 I2C Address			
J21	A0-A5	OFF	Selects non-default I2C address for PCA9685 (see datasheet)
Board/Function Enable			
J24		ON (all)	Remove jumper to disable individual sections of the board. Removing the "BUFFER" jumper disables bidirectional data buffer U26.
Interrupts - IRQ on Interrupt Expander			
JP7	I2CINT	OFF	Routes the I2C interrupt signal to IRQ7 of the cascade interrupt controller.
JP8	SERINT	OFF	Routes the SERial interrupt signal to IRQ6 of the cascade interrupt controller.
JP9	RTCINT	OFF	Routes the RTC periodic interrupt signal to IRQ5 of the cascade interrupt controller.

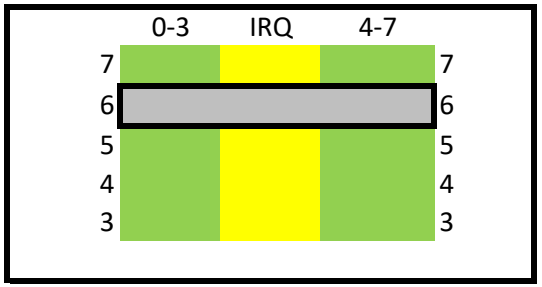
Interrupts - INT for native H8 interrupts



To use H8 INTerrupts, place a jumper over the desired INT line in one of the yellow columns and the matching pin in the source column. The example shows RTC->INT6, SERIAL->INT3, and I2C->INT5



The output from the Cascade Interrupt Controller is sent to one of the native H8 interrupts. IRQ0-3 can be sent to a different H8 INT than IRQ 4-7. The example shows IRQ 0-3 to INT6 and IRQ 4-7 to INT5.
Construct a 1x3 shorting jumper if you want all eight cascade channels to go to a single INTx.



The example shows IRQ 0-7 all routed to H8 INT6