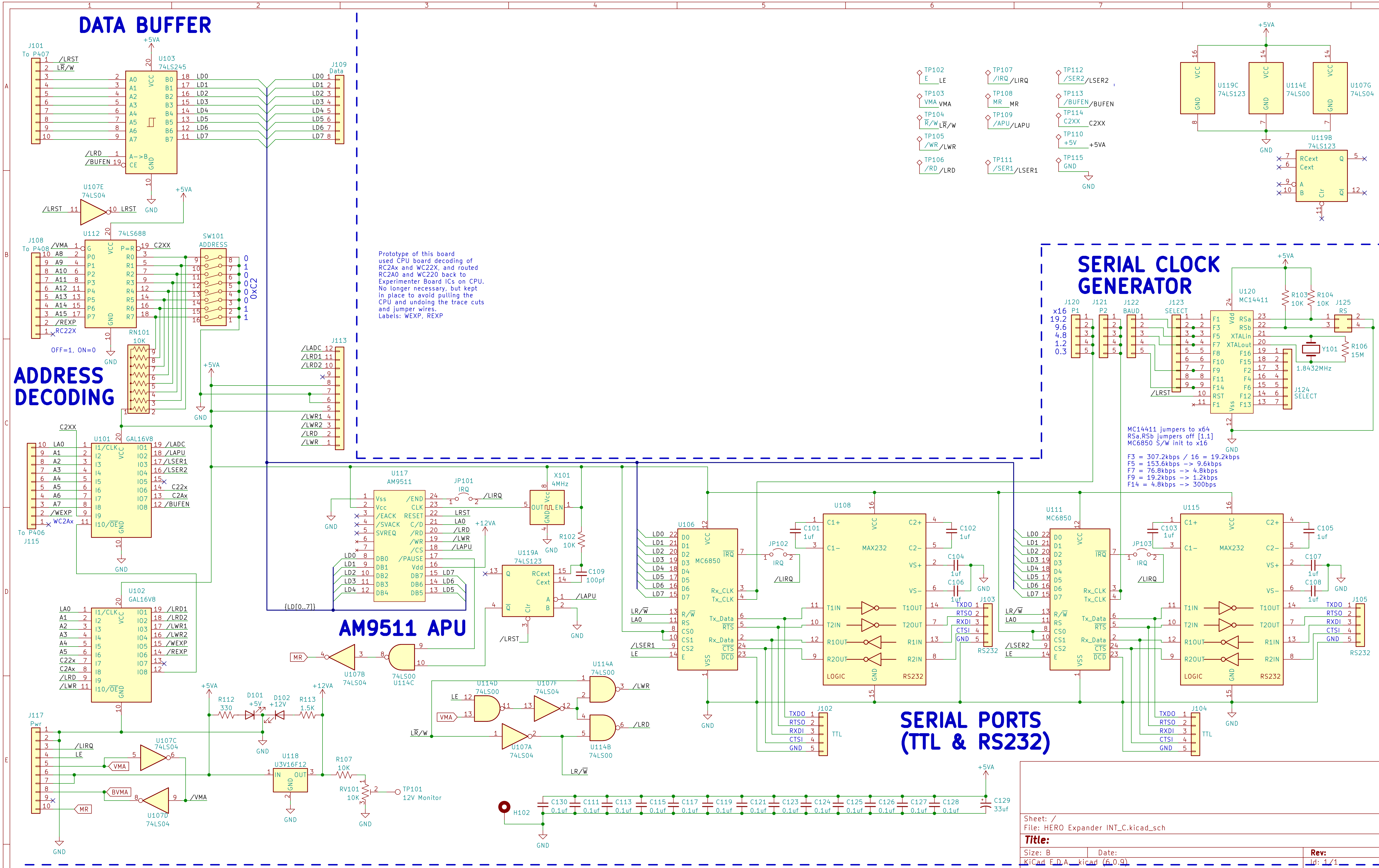
DATA BUFFER
J101
To P407
/LRST
LR/W
U103
74LS245
J109
Data
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
/LRD
/BUFEN
U107E
74LS04
LRST
U112
74LS688
C2XX
J108
To P408
/VMA
A8
A9
A10
A11
A12
A13
A14
A15
/REXP
RC22X
SW101
ADDRESS
0xC2
OFF=1, ON=0
RN101
10K
ADDRESS
DECODING
J113
/LADC
/LRD1
/LRD2
/LWR1
/LWR2
/LRD
/LWR
Prototype of this board
used CPU board decoding of
RC2Ax and WC22X, and routed
RC2A0 and WC220 back to
Experimenter Board ICs on CPU.
No longer necessary, but kept
in place to avoid pulling the
CPU and undoing the trace cuts
and jumper wires.
Labels: WEXP, REXP
U101
GAL16V8
/LAPU
/LSER1
/LSER2
C22x
C2Ax
/BUFEN
/WEXP
WC2Ax
To P406
J115
U102
GAL16V8
U117
AM9511
JP101
IRQ
/LIRQ
X101
4MHz
R102
10K
C109
100pf
U119A
74LS123
AM9511 APU
U107B
74LS04
74LS00
U114C
MR
J117
Pwr
VMA
BVMA
U107C
74LS04
U107D
74LS04
R112
330
D101
+5V
D102
+12V
R113
1.5K
U118
U3V16F12
R107
10K
RV101
10K
TP101
12V Monitor
U114D
74LS00
U107F
74LS04
U114A
74LS00
U107A
74LS04
U114B
74LS00
TP102 E LE
TP103 VMA VMA
TP104 R/W LR/W
TP105 /WR /LWR
TP106 /RD /LRD
TP107 /IRQ /LIRQ
TP108 MR MR
TP109 /APU /LAPU
TP111 /SER1 /LSER1
TP112 /SER2 /LSER2
TP113 /BUFEN /BUFEN
TP114 C2XX C2XX
TP110 +5V +5VA
TP115 GND
U119C
74LS123
U114E
74LS00
U107G
74LS04
U119B
74LS123
SERIAL CLOCK
GENERATOR
J120 P1
J121 P2
J122 BAUD
J123 SELECT
U120
MC14411
R103 10K
R104 10K
J125 RS
Y101
1.8432MHz
R106 15M
J124 SELECT
x16
19.2
9.6
4.8
1.2
0.3
MC14411 jumpers to x64
RSa,RSb jumpers off [1,1]
MC6850 S/W init to x16
F3 = 307.2kbps / 16 = 19.2kbps
F5 = 153.6kbps -> 9.6kbps
F7 = 76.8kbps -> 4.8kbps
F9 = 19.2kbps -> 1.2kbps
F14 = 4.8kbps -> 300bps
U106
MC6850
JP102
IRQ
U108
MAX232
C101 1uf
C102 1uf
C104 1uf
C106 1uf
J103
RS232
J102
TTL
U111
MC6850
JP103
IRQ
U115
MAX232
C103 1uf
C105 1uf
C107 1uf
C108 1uf
J105
RS232
J104
TTL
TXDO
RTSO
RXDI
CTSI
GND
SERIAL PORTS
(TTL & RS232)
H102
C130 C111 C113 C115 C117 C119 C121 C123 C124 C125 C126 C127 C128
0.1uf
C129
33uf
Sheet: /
File: HERO Expander INT_C.kicad_sch
Title:
Size: B
Date:
Rev:
KiCad E.D.A. kicad (6.0.9)
Id: 1/1